CLAIMS

What is claimed is:

1. A buffer circuit that outputs a bias signal for biasing a cascode LNA, the buffer comprising:

an input emitter-follower stage that receives an input signal and produces the bias signal at an output terminal;

a gain stage coupled to the emitter-follower stage;

a load coupled to the emitter-follower stage; and

a feedback circuit coupled to the load and the gain stage.

2. A bias circuit that outputs a bias signal for biasing an amplifier, the bias circuit comprising:

an input stage that receives an input signal and produces the bias signal at an output terminal that is coupled to a gain stage;

a load coupled to the input stage at a first terminal; and

a feedback circuit coupled between the first terminal and the gain stage.

3. The bias circuit of claim 2, wherein the input stage comprises an emitter-follower input stage.

4. The bias circuit of claim 2, wherein the gain stage comprises a common-emitter gain stage that has a base terminal.

5. The bias circuit of claim 4, wherein the feedback circuit is coupled between the first terminal and the base terminal.

6. The bias circuit of claim 5, wherein the feedback circuit comprises:

first and second diodes; and

a capacitor coupled to the first and second diodes.

7. The bias circuit of claim 2, where in the feedback circuit comprises:

first and second diodes; and

a capacitor coupled to the first and second diodes.

8. The bias circuit of claim 2, wherein the feedback circuit comprises a current source coupled to the gain stage.